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EXAMINER	
YEUNG LOPEZ, FEIFEI	
ART UNIT	PAPER NUMBER
2826	
MAIL DATE	DELIVERY MODE
12/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,833	PEKKARINEN ET AL.	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/17/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 8 and 13 are objected to because of the following informalities: Claim 8 claims "an electroconductive element" being "within the cover element" while claim 13, which indirectly depends from claim 8, claims "the electroconductive element" being "outside said cover element." An element can't be within an element and outside of the same element at the same time. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 8-12, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong et al (US Patent 5,889,308).

4. Regarding claim 1, Hong teaches a semiconductor component, comprising a semiconductor element (layer 106 in fig. 4) encased by a cover element (molding compound (a)) having an integrated electroconductive element comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive element to ground in order to shield the semiconductor element against electrostatic pulses (column 4, lines 1-10).

Fig. 4

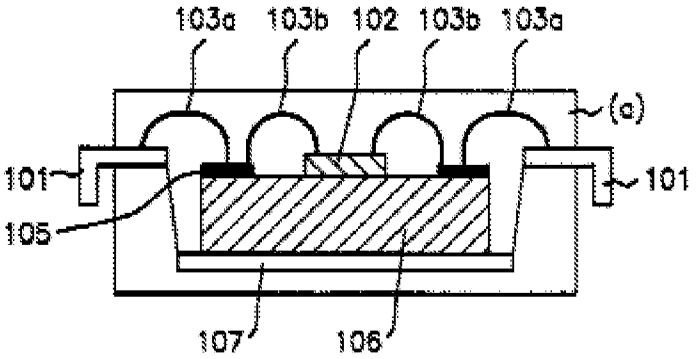


Fig. 5A

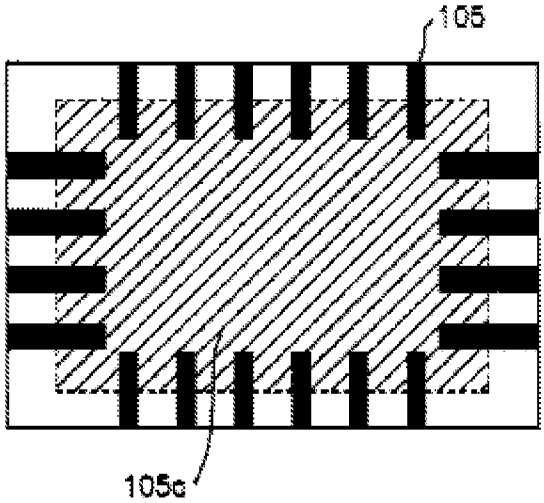
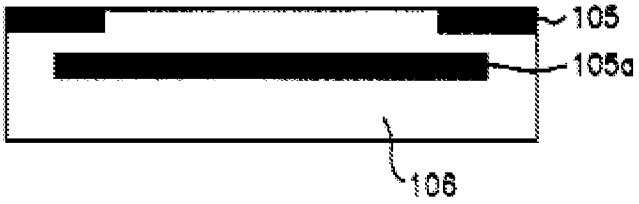


Fig. 5B



5. Regarding claim 2, Hong teaches a semiconductor component according to claim 1, wherein in structure, the electroconductive element is a planar sheet (see figs. 5A and 5B).

6. Regarding claim 3, Hong teaches a semiconductor component according to claim 1, wherein the electroconductive element is a thin loop structure (column 3, lines 34-39).

7. Regarding claim 4, Hong teaches a semiconductor component according to claim 1, wherein the electroconductive element forms a permanent, integrated part of the semiconductor component (fig. 4).

8. Regarding claim 5, Hong teaches a semiconductor component according to claim 1, wherein the electroconductive element is placed underneath the cover element of the semiconductor component, inside said cover element (fig. 4).

9. Regarding claim 8, Hong teaches a method for shielding a semiconductor element (layer 16 in fig. 4) against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component, covering the semiconductor element with a cover element (molding compound (a)), integrating an electroconductive element (layer 106) and providing at least one outlet for the integrated electroconductive element, so that the at least one outlet is configured to connect the electroconductive element to ground (column 4, lines 1-10).

10. Regarding claim 9, Hong teaches a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, planar element (layer 106 in figs. 5A and 5B).

11. Regarding claim 10, Hong teaches a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped element (column 3, lines 34-39).

12. Regarding claim 11, Hong teaches a method according to claim 8, wherein the electroconductive element is integrated as a permanent part of the semiconductor component (fig. 4).

13. Regarding claim 12, Hong teaches a method according to claim 11, wherein the electroconductive element is integrated underneath the cover element of the semiconductor component, inside said cover element (fig. 4).

14. Regarding claim 15, Hong teaches an arrangement including a mounting tray (GND line see fig. 6B for example) and at least one semiconductor component, wherein said at least one semiconductor component comprises a semiconductor element (layer 102 in fig. 4) encased by a cover element (molding compound (a)) having an integrated electroconductive element (layer 106), where the electroconductive element is provided with at least one outlet that is grounded to a ground plane of the mounting tray (column 4, lines 1-10).

15. Regarding claim 16, Hong teaches apparatus for shielding a semiconductor element (layer 102 in fig. 4) against electrostatic pulses, comprising: means for covering (molding compound (a)) the semiconductor element in a semiconductor component having an integrated electroconductive element (layer 106); and means for providing at least one outlet for the integrated electroconductive element, so that the at least one

outlet is configured to connect the electroconductive element to ground (column 4, lines 1-10).

16. Regarding claim 17, Hong teaches the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, planar element (see figs. 5A and 5B).

17. Regarding claim 18, Hong teaches the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped element (column 3, lines 34-39).

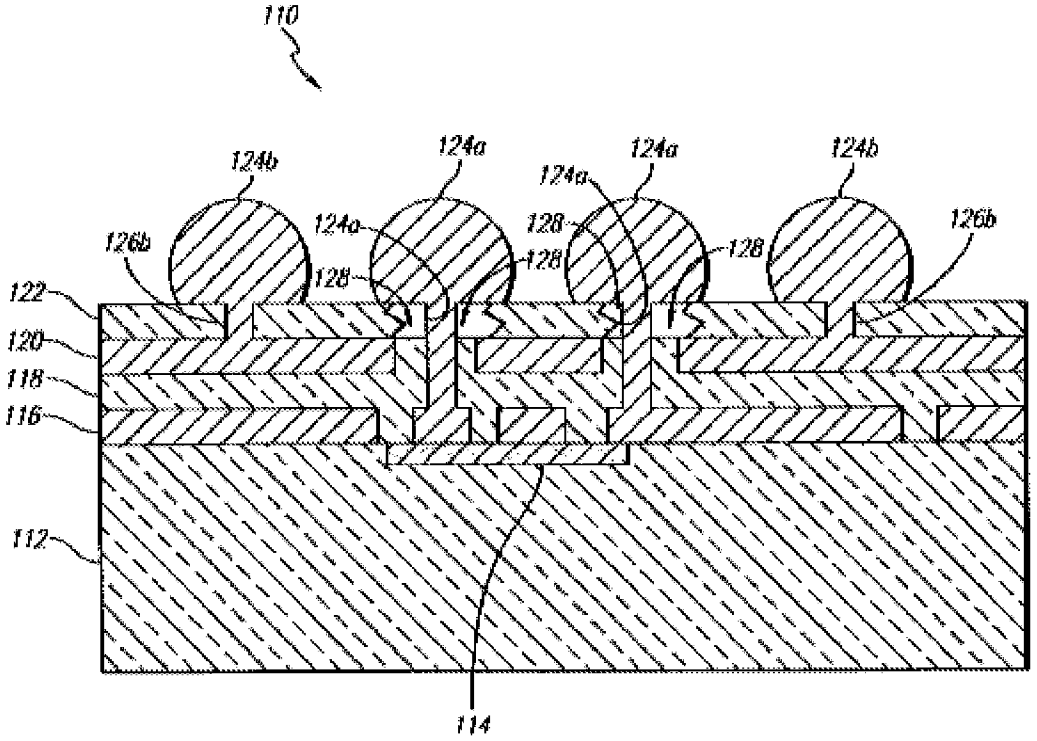
18. Regarding claim 19, Hong teaches the apparatus of claim 16, wherein the electroconductive element is integrated as a permanent part of the semiconductor component (fig. 4).

19. Regarding claim 20, Hong teaches the apparatus of claim 16, wherein the electroconductive element is integrated underneath the cover element of means for covering the semiconductor component, inside said cover element (fig. 4).

20. Claims 1, 6, 8, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hively (US Patent 5,955,762).

21. Regarding claim 1, Hively teaches a semiconductor component, comprising a semiconductor element (layer 114 in fig. 1) encased by a cover element (layer 118) having an integrated electroconductive element comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive element to ground (element 120) in order to shield the semiconductor element against electrostatic pulses (column 3, lines 42-49).

FIG. 1



22. Regarding claim 6, Hively teaches a semiconductor component according to claim 1, wherein the electroconductive element is attached to the cover element of the semiconductor component, outside said cover element (fig. 1).

23. Regarding claim 11, Hively teaches a method according to claim 8, wherein the electroconductive element is integrated as a permanent part of the semiconductor component (fig. 1).

24. Regarding claim 13, Hively teaches a method according to claim 11, wherein the electroconductive element is integrated by attachment to the cover element of the semiconductor component, outside said cover element (fig. 1).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

27. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hively (US Patent 5,955,762) as applied to claims 1 and 8 above, and further in view of Lu et al (PG Pub 2002/0191270 A1).

28. Regarding claim 7, Hively remains as applied in claim 1. However, Hively does not teach electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically. In the same field of endeavor, Lu teaches a polymer layer being induced electrochemically for the benefit that the layer conduction property can be varied by dopant concentration (paragraph

[0006]). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to induce Hively's polymer layer 122 (see column 3, lines 46-49) electrochemically for the benefit that the conduction property, or the minimum voltage at which the polymer becomes conductive, of the layer can be varied by dopant concentration.

29. Regarding claim 14, Hively remains as applied in claim 8. However, Hively does not teach electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically. In the same field of endeavor, Lu teaches a polymer layer being induced electrochemically for the benefit that the layer conduction property can be varied by dopant concentration (paragraph [0006]). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to induce Hively's polymer layer 122 (see column 3, lines 46-49) electrochemically for the benefit that the conduction property, or the minimum voltage at which the polymer becomes conductive, of the layer can be varied by dopant concentration.

Response to Arguments

30. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FYL

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Examiner, Art Unit 2826

/Sue A Purvis/
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